Ultra-Low Power Chip-to-Chip Communications

Project Proposal

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**Abstract:** *This work presents a novel ultra-low power chip-to-chip communications interface designed for low throughput applications running on energy constrained platforms. It targets system power reduction in applications where effective throughputs range from 1kBaud to 1MBaud and can be further optimized for half-duplex operation. This interface is in many ways designed as an answer to the needs of low power designers working in ultra-long lifetime or battery-less contexts.*

# Introduction to the Problem and Motivation

The designers of ultra-low power, resource-constrained computational platforms, such as microcontrollers (MCUs) and application specific integrated circuits (ASICs), often approach reduction of system power consumption during operation with a holistic approach. To this end, a great deal has been done to reduce the power of standard high-end analog and digital circuits. However, chip-to-chip communication structures have yet to become the focus of much of this work, as they typically do not dominate current power budgets.

For this reason, most prior work in the field of chip-to-chip communications focuses on ultra-high throughput applications, in which communication consumes a bigger part of the overall power budget. In these areas throughput-to-pin ratios in the Gbps/pin are suggested [3]. However, when maximum effective throughput-to-pin ratios enter the kbps/pin and below, different design decisions need to be made.

As designers push individual circuits [6] and entire systems on chip (SoCs) [1] [7] to new power lows, the low throughput chip-to-chip communication problem becomes a more interesting one. With average duty-cycled system powers in the range of nano and pico watts [1], a new generation of devices capable of operating under power constraints prohibitive to many standard-complaint serial chip-to-chip protocols will now be enabled for expansion by the creation of a new low-power, low-throughput solution.

# Approach and Figures of Merit

## State of the Art

Currently the problem of low throughput chip-to-chip communication is largely addressed through serialized connections [9] [10]. By reducing pin count and therefore reducing the number of buffers driving wire and trace capacitance, these interfaces minimize energy in low-throughput scenarios [5]. The universal asynchronous receiver/transmitter (UART), inter-integrated circuit (I2C), and serial peripheral interface (SPI) protocols are all examples of common commercialized hardware standards. Though all three protocols are used in low power applications, each has its disadvantage for ultra-low power operation.

UART typically requires baud rate generation in both the master and the slave device. Since no clock is shared between these devices the slave is also responsible for having circuitry fast enough to, upon receiving the masters start bit, begin baud rate generation and start latching in the incoming data on the following baud edge.

I2C is the most power-hungry of the three protocols, and for a somewhat non-obvious reason. The I2C protocol does not use an active pull-up network for driving the bus high; instead, a set of two pull-up resistors are used to pull the bus high as might be done in RTL logic [10]. The result is that nearly the full I2C swing voltage is applied across the pull-ups whenever a zero is passed on the bus. Typical I2C pull-up values are in the range of 10-100kΩ, as further increasing pull-up values tends to result in slower maximum transfer speed, and no further energy reduction.

SPI is typically the lowest power of the three protocols. Because it uses a shared clock line, only the master is responsible for baud rate generation. In addition, its internal hardware is incredibly low complexity [9], and therefore can be made to operate at very low powers. The distributed chip select (slave select) method used by SPI is its biggest downfall, requiring one additional line for each chip on the bus, and increasing pad count in the master.

Most inter-chip communications solutions are evaluated upon the energy-per-bit figure of merit. This figure describes how much energy the bus requires to transmit a single bit of data (assuming the bus changed state for this bit), or the average energy over an even entropy input bit stream. Common state of the art energy-per-bit figures are in the range of 1-100 pJ/bit [4].

We begin by studying the following equations for power and energy per bit to better understand how circuit capacitance, voltage, and leakage knobs needed to be turned to reduce the power consumption and energy per operation, both when in operation and idling.

Equation 1: Energy per bit derivation

It is worth noting that energy per bit is minimized as effective throughput grows large, or input stream entropy grows low, due to the leakage for low throughput dominating the energy consumption (see Figure 1). This means the most efficient operation occurs where system throughput is high (we cannot control this knob) so an alternative figure of merit for low-throughput systems may be derived.

Figure 1: Energy per bit versus throughput plot

## Approach and Contributions

The first and most straight-forward decision is to base the design around the SPI model instead of the I2C or UART. This is because the use of pull-up resistors I2C results in high static current during low bit periods, severely limiting its usefulness in an ultra-low power environment. UART baud rate generation can also dominate system consumption if not carefully managed during otherwise inactive periods.

Energy increases proportionally to VIO \* Vswing, the product of I/O voltage and output swing, which translates to VIO2 given full swing operation. Thus decreasing VIO results in a quadratic reduction of energy required to transmit a bit as shown in Equation 1. Unfortunately, this also presents two new problems. As VIO approaches the threshold voltage, the operation of the transistors slows, decreasing the upper limit on the frequency of operation. In addition, efficient power gating structures for large devices, such as buffers that might operate from sub-threshold to far super-threshold (3.3V compliance) is a unique challenge. By exploiting the balance of required throughput during operation and leakage reduction in sleep mode, significant power reduction is possible.

Ideally, by tuning both of these knobs, we will be able to find an optimally energy efficient frequency of operation for our circuit. Finding this optimal operating point is further complicated by the existence of an activity factor during transmission, as the data line will not be changing every clock cycle. In addition, the transmission line is not constantly functioning, as data does not need to be transmitted at all times. Lastly, activity factor can be decreased by using a technique that reduces the amount of switching that occurs in transmission, effectively pushing the optimal operating frequency up.

By turning off the circuit when not in use, we can reduce power consumption, as there is a leakage current through each gate while idling in full power mode. This can be done through power gating the logic in the circuit with a PMOS connected to the pull up network or an NMOS connected to the pull down network, or both. However, this has other effects on the operation of the circuit.

We plan to further our investigation into the effects of these factors, quantizing the optimal values from the equations using values from our particular circuit. This investigation comprises the research contribution of the work.

# Project Design Stages and Schedule

In order to help better arrange the project and enforce meeting deadlines in a timely manner, five primary project stages are established. These are as follows:

1. Modeling and design-space-exploration
2. Power management and reduction
3. Bus arbitration and system control
4. System integration and support
5. Verification, iteration, and refinement

In the following stage descriptions the design and novelty of the project is introduced.

### Stage 1: Design Space Exploration

In the first stage of design, the simplest possible system fulfilling the specification of serialized chip-to-chip communication is designed. This consists of only two drivers, a shift register, and a simplified pad/PCB trace model. Novel components include a sub/super-threshold driver design and shift register optimized for low-leakage shutdown operation.

Before the first design review models of the chip-to-chip communications channel and simplistic buffer were created. These models were then used for evaluation of the most critical powers in the physical layer.

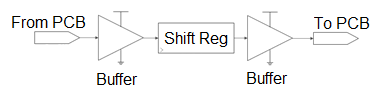


Figure 2: Simple Physical Layer Implementation

\*\*New simulation results for a more complicated and realistic driver structure are included in an appendix to this document.

### Stage 2: Power Management and Reduction

In stage two, power management and reduction techniques are considered. Here, the focus is on design for the physical layer. Structures such as headers for effective power gating, increased stacks for leakage reduction and driver design for low output swing provide a majority of the improvements. Novel contributions include power management topologies for a wide range of output swings and low- power, fast wake-up retention modes for shift register design.

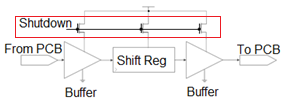


Figure 3: Physical Layer Power Reduction

### Stage 3: Bus Arbitration and Control

In stage three, we will design bus arbitration blocks, allowing us to monitor the number of bits sent to/received from the bus and a control register for actuating system operation based on these values. It is worth noting that this arbitration block may be synthesized from Verilog depending on its power, determined relative to buffers and the shift register. The novel contribution of this stage will likely be contingent on optimizing control logic for the unique parameters of the aforementioned physical design.

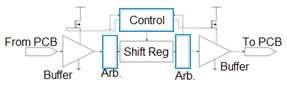


Figure 4: Control actuation and Bus Arbitration

### Stage 4: System Integration

In stage four, an additional suite of registers and control logic is added to the block in order to improve ease of integration with existing architectures. This includes the addition of interrupts, transmit and receive buffers, and flexible clocking for baud rate generation. Relatively little of this design will be novel, as it is intended for easy integration with common practice in academia and industry.

This design will most likely be largely implemented in synthesized Verilog and simulated behaviorally. SPICE simulation will later be used for power/energy extraction.

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Figure 5: Integrated Module Structure

### Stage 5: Iterative Improvement

In the final stage we will take additional knowledge gained during the previous 3 stages and apply it recursively to the first stage of the design process. In this way we attempt to assure that we will not miss out on key power optimizations that may have not been initially obvious upon approaching the problem from a less informed stance on the issue.

## Schedule

The preliminary scheduling for the five design stages, as described previously, is summarized in the Gantt chart below. A portion of the first stage was completed as part of the first design review.

Figure 6: Preliminary Schedule

## Task Breakdown

Up to now Ben has primarily worked on driver design and the physical channel model (pad and PCB trace modeling). Chris has worked on shift register design and power profiling for power-gated driver structures.

Moving forward, preliminary results indicate both members will be involved in the driver design process. Shift register topology may not be considered as closely, but Chris will manage register design and bus arbitration. Ben will focus on buffer and pad integration and architecture for interfacing a peripheral bus.

# Anticipated Outcomes

Though we are relatively far through the design exploration stage it is still somewhat difficult to anticipate final outcomes. As an effort to help set realistic goals we have created two lists of goals which are included below.

## Intermediate Outcomes

* Evaluation of the E/b figure of merit for low-throughput communications
* Determination of a new/modified figure of merit for ultra-low power shutdown systems
* Attempt to optimize this work for the derived figure of merit
* Complete design of an efficient shift register and driver structure in IBM 130nm technology

## Final Outcomes

* Create a custom circuit using low (possibly sub-VT) VDD for the logic and flexible VIO for the I/O operation
* Design a chip-to-chip communications circuit that is at least an order of magnitude lower power than a standard SPI at 3.3V
* Minimize the activity factor on the I/O to reduce energy by modifying the transmission protocol
* Further reduce power by introducing a mode of operation that gates the circuit’s logic and I/O while retaining register data and reducing leakage (sleep).

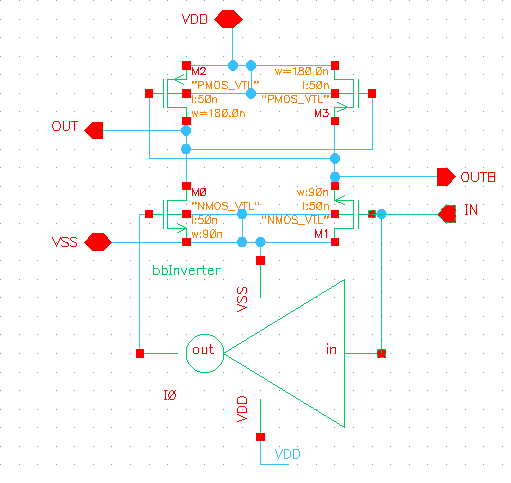
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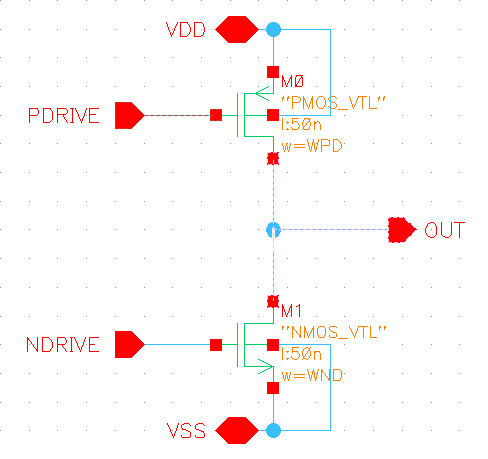
# Appendix: Additional Simulation Results

A more practical driver design was implemented and simulated in FreePDK 45nm technology to demonstrate functionality. All future designs and simulation will be carried out in IBM 130nm technology.

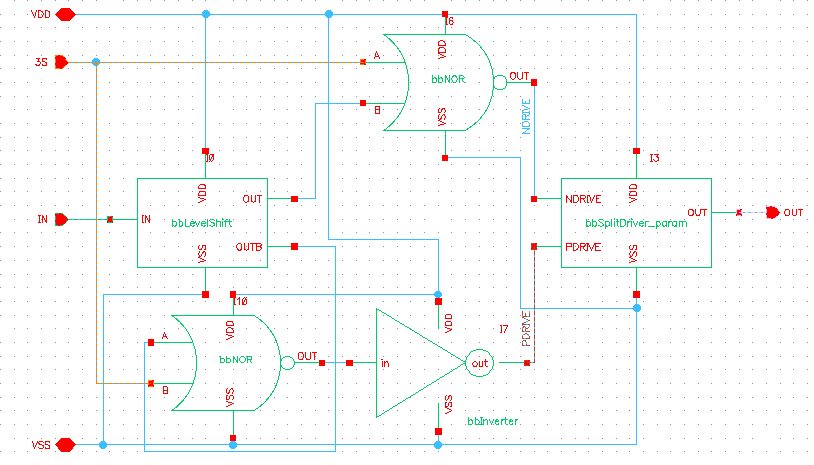
**Simple Level Converter**



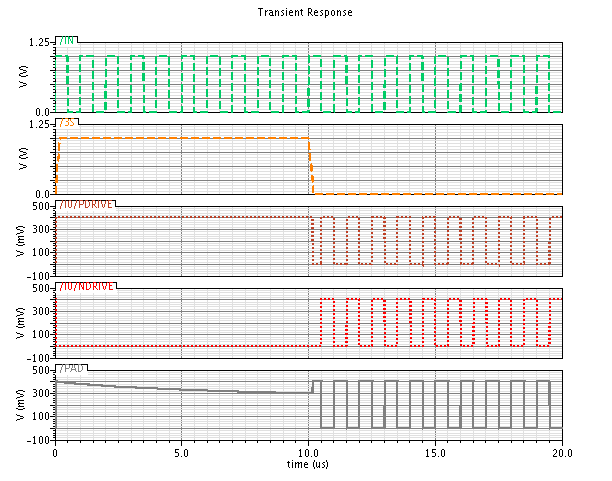
**Split-Driver Final Driver Stage (allows for tri-state control)**



**Final Driver Design (w/ tri-state)**

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**First Driver Simulation Result**

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